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I further certify that the annexed documents are not, as yet, open to public inspection.

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WITNESS my hand this Eighth day of April 1994.

DAVID DANIEL CLARKE
DELEGATE OF COMMISSIONER OF PATENTS

DATA SWITCH FOR ASYNCHRONOUS TRANSFER MODE-BASED NETWORKS

AUSTRALIAN
PROVISIONAL No. PL7981
DATE OF FILING 26 MAR. 93
PATENT OFFICE

Technical Field

This invention relates to the multiplexing and switching of data frames within digital communication systems which employ label multiplexed cells and the Asynchronous Transfer Mode of mulitplexing, transmission and switching. One manifestation of the Asynchronous Transfer Mode referred to in this field description is that envisaged by the International Telecommunications Union for its Broadband Integrated Services Digital Network.

Background of the Invention

The telephone industry is moving within the Standardisation Sector of the International Telecommunications Union to define the concept of a Broadband Integrated Services Network or B_ISDN. This Broadband Integrated Services Network is to be capable of providing a complete range of services, from telephone through television to data, with all services being multiplexed onto the network over a defined User Network Interface (UNI). Switches within the network are interconnected over a defined Network Node Interface (NNI).

Information for all services within the Broadband Integrated Services Network is conveyed and switched in irregularly occurring fixed size segments called cells, with the method of cell handling referred to as the Asynchronous Transfer Mode (ATM). ATM is a connection oriented technique where ATM level connections are established between service users by means of a call set up or signalling process, or alternatively administratively by network management. Connections may be established for the duration of a call or information transfer, or they may be established on a permanent or semi-permanent basis. The ATM cell has a header block which carries the label necessary to associate cells belonging to the same virtual connection.

In terms of protocol architecture the ATM layer, which sits immediately above the physical or transmission layer, has two hierarchical levels. These are the lower Virtual Path level (VP) and the higher Virtual Channel level (VC). The Virtual Channel describes the unidirectional flow of ATM cells marked by a unique identifier, carried in the cell header, called the Virtual Channel Identifier (VCI) and belonging to Virtual Channels associated by a common unique identifier, carried in the cell header, called the Virtual Path Identifier (VPI). Virtual Channels are transported within Virtual Paths which are used to aggregate Virtual Channels. The use of Virtual Paths facilitates transit switching and can also provide, among other uses, a means of associating Virtual Channels carrying the same type of service.

In accepting connections over the B_ISDN the network operator needs to confirm that sufficient network resources are available to sustain the connection end to end at its required Quality of

Service and without affecting the service guarantees of the existing connections. To assist in the process of Connection Admission Control the network user is required to characterise its traffic and specify the required Quality of Service. Source traffic may be characterised by its average bit rate, peak bit rate, burstiness, peak duration and other such measures. If a required connection can be resourced it would be accepted by the network which would then monitor the traffic flow to ensure that the agreed traffic parameters are not violated. ATM related Quality of Service is to be rated in terms of such parameters as the end to end cell transfer delay, cell delay variation, cell loss ratio and cell error ratio. Because of the need to bound cell delay on an end to end basis delay budgets would apply over local, regional, national and international areas. Accordingly ATM switches offering either virtual path or virtual path and virtual channel switching are expected to employ small buffers of no more than several hundred cell capacity with the switch loading kept at such a level as to ensure acceptable cell loss levels through buffer overflow. Switch loading is a parameter which is managed through such means as call admission control, exercised on prospective new connections, and the enforced scheduling of traffic flows on existing connections according to the negotiated parameters. To provide a data service for N end users over the ATM network one may in the extreme envisage the use of a set of N(N-1) fully meshed and bandwidth resourced connections. Any departure from full meshing requires users to share connections in a statistically multiplexed basis and network nodes which offer such a multiplexing service. Such multiplexing is currently envisaged as being at a protocol level above the ATM level. This could be at the ATM Adaption Layer (AAL), or even higher. For data services there are several different AAL layers which may be used and these provide among other functions a segmentation and reassembly service wherein data frames from higher layers are mapped into ATM cells and vice versa. Multiplexing data frames involves the use of buffers that are much larger than those used within ATM switches since these are required to smooth the data flow peaks associated with data flowing from multiple bandwidth resourced tributaries into a single resourced tributary. When buffer overflow occurs whole data frames are discarded rather than individual cells originating from different frames as would be the case with ATM level multiplexing.

Summary of the Invention

This invention of the Data Switch enables non bandwidth resourced Virtual Circuits, carried within bandwidth resourced input Virtual Path connections, to be cross connected or switched into bandwidth resourced output Virtual Paths. With existing techniques statistical multiplexing of user data is only possible within a bandwidth resourced connection and such connections are to other users or to a network node which provides a multiplexing service at the AAL level or above. The Data Switch however operates at the ATM level.

The Data Switch invention is described here in the context of the B_ISDN ATM network. The invention is however not limited in scope and applies to any ATM-based network whether public or private, local or wide area.

Brief Description of the Drawings

The invention should become fully apparent when taken in connection with the following detailed description and accompanying drawings in which:

Figure 1 shows the ATM cell structure
Figure 2 shows the cell header at the UNI
Figure 3 shows the cell header at the NNI
Figure 4 shows the B_ISDN layered architecture
Figure 5 shows the Virtual Path Switch
Figure 6 shows the Virtual Channel switch
Figure 7 shows the general model of a VP or VC switch
Figure 8 shows the Data Switch
Figure 9 shows the VP Server element of the Data Switch
Figure 10 shows the flow diagram of the machine which controls the discarding of data frames in the VP Server buffer.

Detailed Description

With ATM all information to be transferred across the B_ISDN UNI or NNI is packed into fixed sized segments called cells. As shown in Figure 1 these cells have a 48 octet information field and a 5 octet header. The ATM cell header block contains the VPI and VCI fields which carry the labels necessary to associate cells belonging to the same Virtual Path and Virtual Circuit respectively. Figures 2 and 3 show the location and size of these fields for the respective UNI and NNI.

The protocol reference model for the B_ISDN is illustrated in Figure 4. Here the lower or Physical layer is responsible for the transmission and reception of ATM cells over one of a variety of transmission media and transmission systems. Above the Physical Layer is the ATM layer which comprises the Virtual Path and Virtual Circuit sublayers. Here cells from individual VPs and VCs are multiplexed into a composite stream for transmission, and arriving cells split into individual tributaries according to the appropriate VP and VC. The ATM Adaption layer sits above the ATM layer and is responsible, among other functions, for the mapping of large data frames into the ATM cell payloads and vice versa.

Virtual Path and Virtual Circuit cell streams are switched within the ATM network. As shown in Figure 5, VP switches terminate incoming VP connections and cross-connect incoming VPIs to outgoing VPIs according to the required destinations. The VPI may be reassigned in the switching process but the VCs within each VP remain intact with the VCI values remaining unchanged. A VC switch on the other hand terminates both VC and VP connections and switches the VCs within a VP independently of each other. The VC switch can translate both VPIs and VCIs as illustrated in Figure 6. Because of switching within the ATM network the VPI and VCI values associated with a particular connection may be different at the two ends.

ATM switches, or cross-connecting nodes, are seen from the above descriptions to perform two main functions: the transport of cells from their inputs to their dedicated outputs, and the translation, where relevant, of cell VPIs and VCIs. Accordingly ATM switches are in general made up of an interconnection network and an input and output controller for each incoming and outgoing line respectively. The arrangement is as shown in Figure 7. Here cells arriving at each input controller are synchronised to an internal clock used by the switch. This clock operates at a

rate higher than the input line rate. The output controller transports cells, which have passed through the interconnection network towards their destinations. To avoid cell loss caused by two or more cells simultaneously competing for the same output, buffers have to be provided. These may be located at the input or output controllers or form part of the interconnection network. Because the ATM switches are to be deployed in switching resourced connections with small throughput delay the associated buffers would be of no more than on the order of a hundred cell capacity.

Figure 8 shows a logical schematic of the Data Switch which is useful in describing the principles of the invention. The Data Switch incorporates VP Servers and essentially enables non bandwidth resourced VCs, carried within bandwidth resourced input VPs, to be crossconnected or switched into bandwidth resourced output VPs. With existing techniques statistical multiplexing of user data is only possible within a bandwidth resourced connection and such connections are to other users or to a network node which provides a multiplexing service at the AAL level or above. The Data Switch however operates at the ATM level. It employs a normal VP and VC front end switching stage to deliver the non bandwidth resourced VCs to the VP Server. The VP switch terminates the VPs and feeds a single VP onto each input line of the VC switch. The VC switch cross-connects and multiplexes the non-bandwidth resourced VCs onto single output VPs which provide the inputs to the VP server. Cells are extracted from the VC switch at such a rate as to not overflow its own output buffers. The VP server, shown in Figure 9, which is useful in describing the principles of the invention, comprises large input buffers, to accommodate and smooth the non-bandwidth resourced data traffic carried on the input VCs, and a scheduler to deliver traffic on the output VP according to traffic parameters agreed for that VP. When buffer overflow occurs in the VP server, whole data frames rather than individual ATM cells are discarded. For this to be possible at the ATM level the cell headers must carry delimeters to mark the position of the end of frame, and individual cells on a frame must be carried contiguously on a given VC. One particular ATM Adaption Layer, i.e. AAL5 defined for the B_ISDN, currently offers such frame marking at the ATM level.

Figure 10, which is useful in describing the principles of the invention, shows the flow chart of one realisation of a machine which controls the discarding of data frames in a VP Server buffer. Its modus operandi is such that when the buffer cell occupancy exceeds a specified threshold newly arriving data frames, other than those which fit entirely into the payload of single cell, are discarded. A different realisation may discard even the single cell frames when the buffer threshold is exceeded. Yet another realisation may operate either of the above threshold strategies and in addition may discard existing whole data frames from within the buffer at overflow or partially complete data frames whose first cell is within the buffer but whose last cell is yet to arrive. An example of the realisation of the Scheduler within the VP Server is a device which extracts cells from the VP Server buffers at a constant fixed rate. This device is appropriate for VP traffic flows which are to be characterised by their peak rate with this peak rate being also the enforced rate. In this instance the peak rate and the extraction rate would be the same. Different types of Schedulers would apply to other required traffic characterisations by other than by peak rate.

When Data Switches as described in this invention would be employed within ATM networks of the B_ISDN the entry of user data frames from protocol levels above the ATM layer of the UNI

would require either the mapping of data frame addresses onto the (unresourced) VCIs, or the mapping of frame datalink connection identifiers onto the (unresourced) VCIs. The former would apply to connectionless data services and the latter to such connection oriented data services as Frame Relay. Within the ATM network the bandwidth unresourced VCIs would be carried within bandwidth resourced VPIs from Data Switch to Data Switch and on to their final destinations..

We note that the data switch may be used to switch also bandwidth resourced VPIs and VCIs for which the VP server function would be null. Moreover, the data switching capability may be implemented in only a part of a standard ATM switch. If the ATM switch has multicast capabilities, wherein an input cell can be switched to more than one output, multicasting becomes a capability also of the data switch.

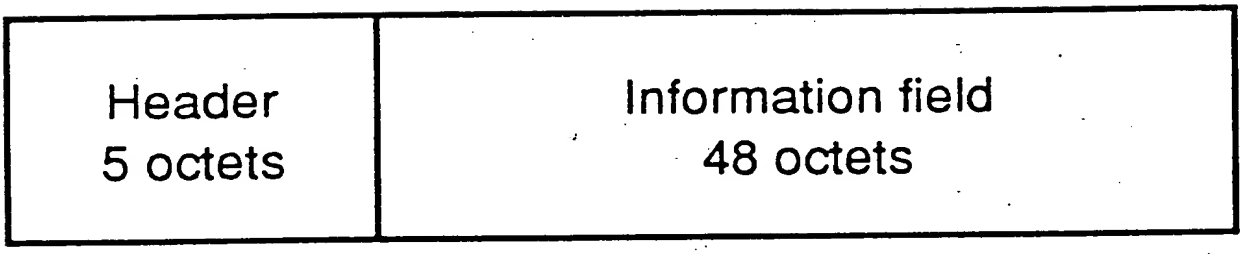


FIGURE 1

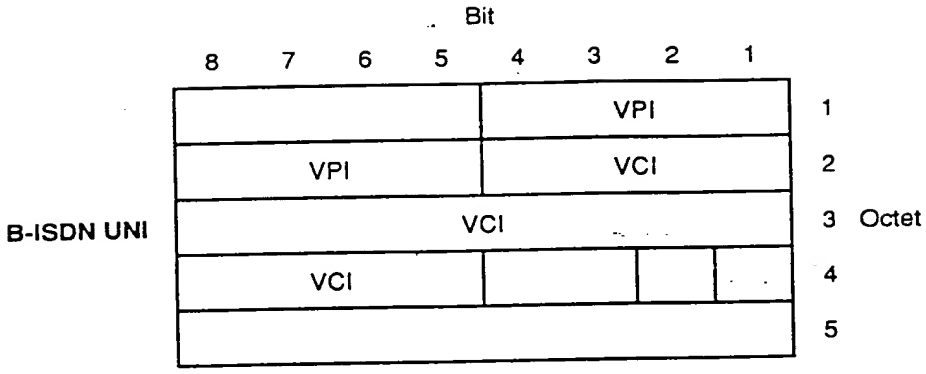


FIGURE 2

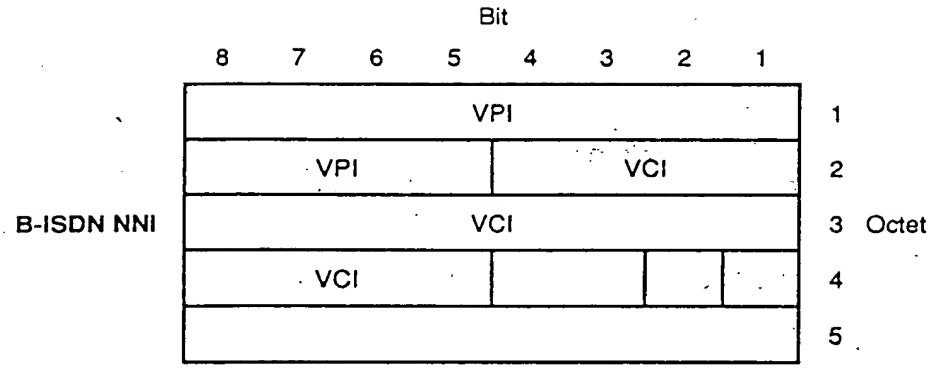


FIGURE 3

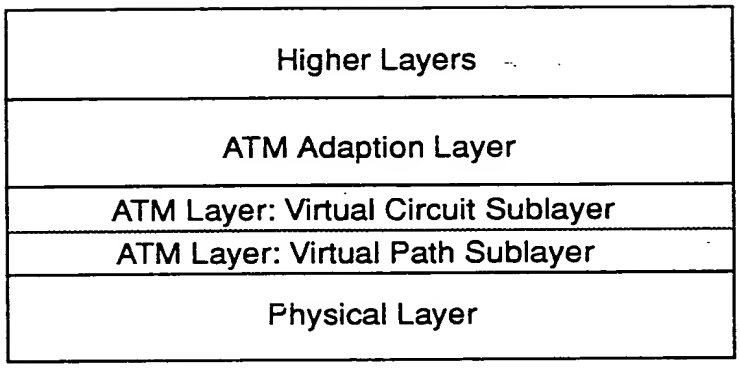

Higher Layers
ATM Adaption Layer
ATM Layer: Virtual Circuit Sublayer
ATM Layer: Virtual Path Sublayer
Physical Layer

FIGURE 4

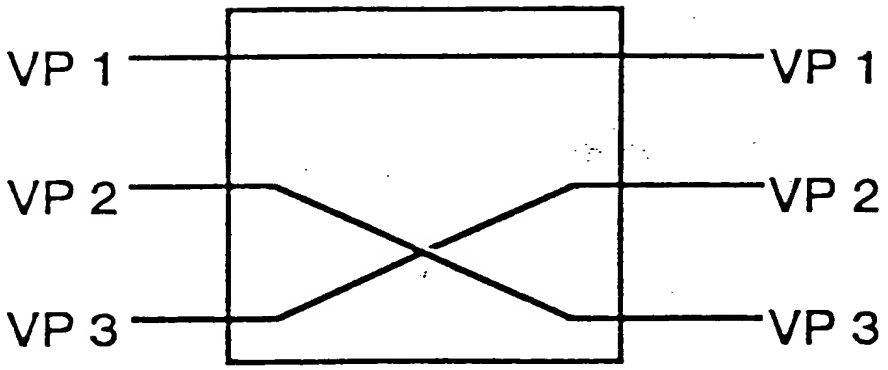


FIGURE 5

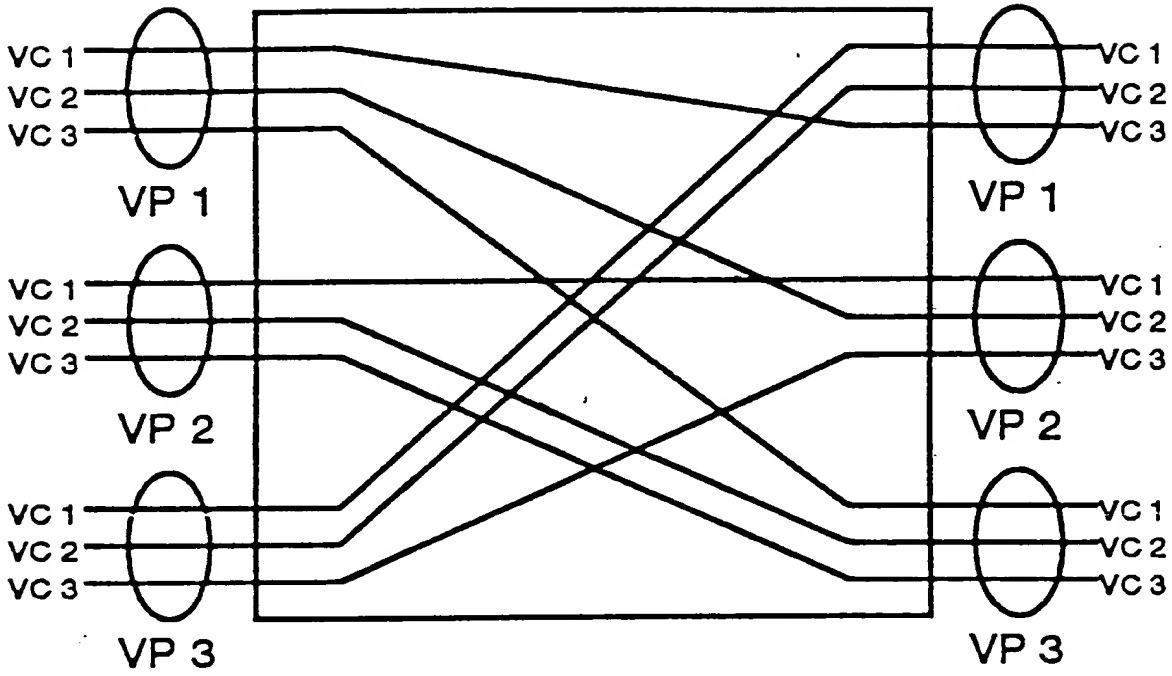
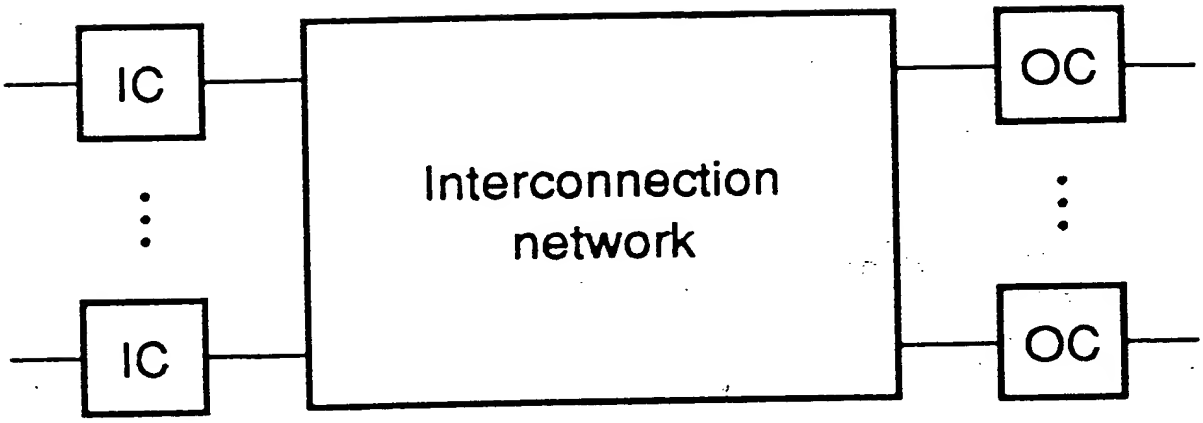

VC 1
VC 2
VC 3
VP 1
VC 1
VC 2
VC 3
VP 2
VC 1
VC 2
VC 3
VP 3
VC 1
VC 2
VC 3
VP 1
VC 1
VC 2
VC 3
VP 2
VC 1
VC 2
VC 3
VP 3

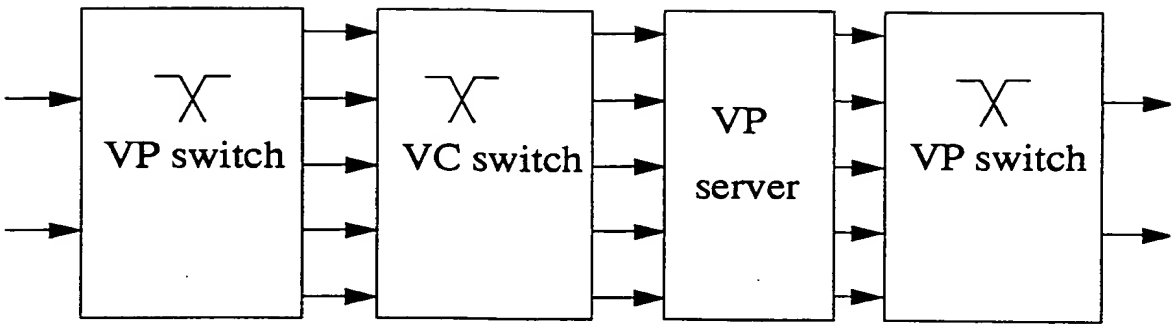
FIGURE 6



IC Input controller
OC Output controller

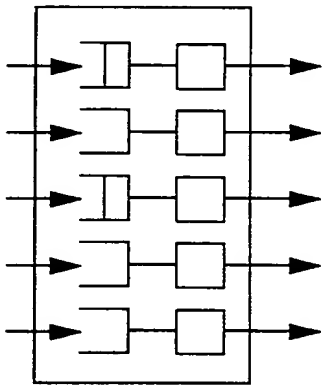
FIGURE 7

FIGURE 8



Frame Data Switch (FDS)

FIGURE 9



VP Server

Scheduler

Note:
'BOM' Beginning of Frame
'EOM' End of Frame

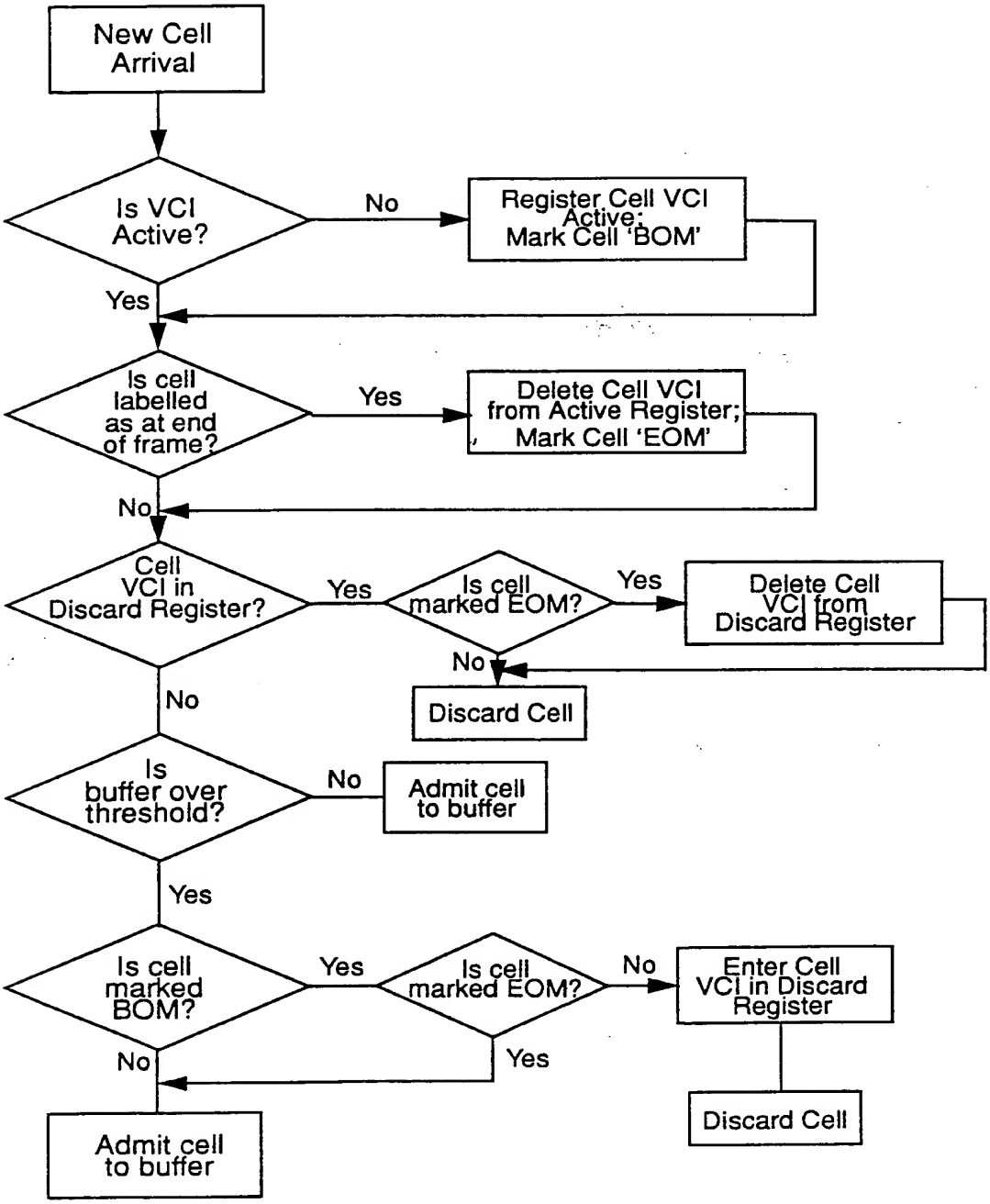


FIGURE 10